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NOTICE OF ALLOWANCE AND FEE(S) DUE

23117 7590 10/09/2008

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/09/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,575	06/24/2003	Martin Robert Evans	550-445	8224

TITLE OF INVENTION: SYNCHRONISATION BETWEEN PIPELINES IN A DATA PROCESSING APPARATUS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/09/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23117 7590 10/09/2008

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,575	06/24/2003	Martin Robert Evans	550-445	8224

TITLE OF INVENTION: SYNCHRONISATION BETWEEN PIPELINES IN A DATA PROCESSING APPARATUS

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nonprovisional	NO	$1510	$300	$0	$1810	01/09/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CHUN KUAN	2181	712-034000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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EXAMINER	
LEE, CHUN KUAN	
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2181	

DATE MAILED: 10/09/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 516 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 516 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/601,575	EVANS ET AL.	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/16/2008*.

2. ☒ The allowed claim(s) is/are *1-22,24,25,27-39,41,42,44 and 45*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. In view of the appeal brief filed on 07/16/2008, PROSECUTION IS HEREBY REOPENED. The allowance of the claims is set forth below.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

I. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

3. Authorization for this examiner's amendment was given in a telephone interview with John Lastova, having Reg. No. 33,149, on 10/02/2008. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

NOTE: The claims amended by this examiner's amendment have been referred to by their original claim number.

4. In claim 1, "A data processing apparatus, comprising:

a main processor configured to execute a sequence of instructions, the main processor comprising a first pipeline having a first plurality of pipeline stages;

a coprocessor configured to execute coprocessor instructions in said sequence of instructions, the coprocessor comprising a second pipeline having a second plurality of pipeline stages, and each coprocessor instruction being arranged to be routed through both the first pipeline and the second pipeline; and

at least one synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries and coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines, the predetermined pipeline stage being configured to cause a token to be placed in an entry of the synchronizing queue when processing a coprocessor instruction, the token including a tag which uniquely identifies the coprocessor instruction to which the token relates, and the partner pipeline stage being configured to process that coprocessor

instruction upon receipt of the token from the synchronizing queue, thereby synchronizing the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage without passing signals with fixed timing between the pipelines"

is replaced with -A data processing apparatus, comprising:

a main processor that executes a sequence of instructions, the main processor comprising a first pipeline having a first plurality of pipeline stages;

a coprocessor that executes coprocessor instructions in said sequence of instructions, the coprocessor comprising a second pipeline having a second plurality of pipeline stages, and each one of the coprocessor instructions being arranged to be routed through both the first pipeline and the second pipeline; and

at least one synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries and coupling a predetermined pipeline stage in one of the first or second pipeline with a partner pipeline stage in the other one of the first or second pipeline, the predetermined pipeline stage placing a token in an entry of the synchronizing queue when processing one of the coprocessor instructions, the token including a tag which uniquely identifies said one of the coprocessor instructions to which the token relates, and the partner pipeline stage processing the corresponding one of the coprocessor instructions upon receipt of the token from the synchronizing queue, thereby synchronizing the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage without passing signals with fixed timing between the first and second pipelines-.

5. In claim 2, "A data processing apparatus as claimed in Claim 1, further comprising a plurality of said synchronizing queues, each said synchronizing queue coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines"

is replaced with -A data processing apparatus as claimed in Claim 1, further comprising a plurality of said synchronizing queues, each of said synchronizing queues coupling the predetermined pipeline stage in one of the first or second pipeline with the partner pipeline stage in the other one of the first or second pipeline-.

6. In claim 3, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is an instruction queue, the predetermined pipeline stage is in the first pipeline and is arranged to cause a token identifying a coprocessor instruction to be placed in the instruction queue, and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token to begin processing the coprocessor instruction identified by the token"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is an instruction queue, the predetermined pipeline stage is in the first pipeline and places the token identifying said one of the coprocessor instructions in the instruction queue, and the partner pipeline stage is in the second pipeline and upon receipt of the token begins processing the corresponding one of the coprocessor instructions identified by the token-.

7. In claim 4, "A data processing apparatus as claimed in Claim 3, wherein the predetermined pipeline stage is a fetch stage in the first pipeline and the partner pipeline stage is a decode stage in the second pipeline, that decode stage being configured to decode the coprocessor instruction upon receipt of the token"

is replaced with -A data processing apparatus as claimed in Claim 3, wherein the predetermined pipeline stage is a fetch stage in the first pipeline and the partner pipeline stage is a decode stage in the second pipeline, said decode stage decoding the corresponding one of the coprocessor instructions upon receipt of the token-.

8. In claim 5, "A data processing apparatus as claimed in Claim 4, wherein the fetch stage in the first pipeline is configured to cause a token to be placed in the instruction queue for each instruction in the sequence of instructions, and the decode stage in the second pipeline is arranged to decode each instruction upon receipt of the associated token in order to determine whether that instruction is a coprocessor instruction that requires further processing by the coprocessor"

is replaced with -A data processing apparatus as claimed in Claim 4, wherein the fetch stage in the first pipeline places the token in the instruction queue for each instruction in the sequence of instructions, and the decode stage in the second pipeline decodes said each instruction upon receipt of the associated token in order to determine whether said each instruction is the corresponding one of the coprocessor instructions that requires further processing by the coprocessor.-.

9. In claim 6, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a cancel queue, the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the cancel queue a token identifying whether a coprocessor instruction at that predetermined pipeline stage is to be cancelled, and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token from the cancel queue, and if the token identifies that the coprocessor instruction is to be cancelled, to cause that coprocessor instruction to be cancelled"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a cancel queue, the predetermined pipeline stage is in the first pipeline and places in the cancel queue the token identifying whether said one of the coprocessor instructions at the predetermined pipeline stage is to be cancelled, and the partner pipeline stage is in the second pipeline and upon receipt of the token from the cancel queue, and if the token identifies that said one of the coprocessor instructions is to be cancelled, to cancel the corresponding one of the coprocessor instructions-.

10. In claim 8, "A data processing apparatus as claimed in Claim 6, wherein the partner pipeline stage is configured upon receipt of the token from the cancel queue, and if the token identifies that the coprocessor instruction is to be cancelled, to remove the coprocessor instruction from the second pipeline"

is replaced with -A data processing apparatus as claimed in Claim 6, wherein the partner pipeline stage upon receipt of the token from the cancel queue, and if the token identifies that said one of the coprocessor instructions is to be cancelled, to remove the corresponding one of the coprocessor instructions from the second pipeline-.

11. In claim 9, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a finish queue, the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the finish queue a token identifying permission for a coprocessor instruction at that predetermined pipeline stage to be retired from the second pipeline, and the partner pipeline stage is in the second pipeline and is configured upon receipt of the token from the finish queue, and if the token identifies that the coprocessor instruction is permitted to be retired, to cause that coprocessor instruction to be retired"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a finish queue, the predetermined pipeline stage is in the first pipeline and places in the finish queue the token identifying permission for said one of the coprocessor instructions at said predetermined pipeline stage to be retired from the second pipeline, and the partner pipeline stage is in the second pipeline and upon receipt of the token from the finish queue, and if the token identifies that said one of the coprocessor instructions is permitted to be retired, to retire the corresponding one of the coprocessor instructions-.

12. In claim 11, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a length queue, the predetermined pipeline stage is in the second pipeline and is arranged, for a vectored coprocessor instruction, to cause to be placed in the length queue a token identifying length information for the vectored coprocessor instruction, and the partner pipeline stage is in the first pipeline and is configured upon receipt of the token from the length queue to factor the length information into the further processing of the vectored coprocessor instruction within the first pipeline"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a length queue, the predetermined pipeline stage is in the second pipeline and places in the length queue the token identifying length information for a vectored coprocessor instruction, and the partner pipeline stage is in the first pipeline and upon receipt of the token from the length queue factors the length information into the further processing of the vectored coprocessor instruction within the first pipeline-.

13. In claim 13, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is an accept queue, the predetermined pipeline stage is in the second pipeline and is arranged to cause to be placed in the accept queue a token identifying whether a coprocessor instruction in that predetermined pipeline stage is to be accepted for execution by the coprocessor, and the partner pipeline stage is in the first pipeline and is configured upon receipt of the token from the

accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to cause that coprocessor instruction to be rejected by the main processor"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is an accept queue, the predetermined pipeline stage is in the second pipeline and places in the accept queue the token identifying whether said one of the coprocessor instructions in the predetermined pipeline stage is to be accepted for execution by the coprocessor, and the partner pipeline stage is in the first pipeline and upon receipt of the token from the accept queue, and if the token identifies that said one of the coprocessor instructions is not to be accepted, to reject the corresponding one of the coprocessor instructions by the main processor-.

14. In claim 15, "A data processing apparatus as claimed in Claim 14, wherein the partner pipeline stage is configured upon receipt of the token from the accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to remove the coprocessor instruction from the first pipeline"

is replaced with -A data processing apparatus as claimed in Claim 14, wherein the partner pipeline stage upon receipt of the token from the accept queue, and if the token identifies that said one of the coprocessor instructions is not to be accepted, to remove the corresponding one of the coprocessor instructions from the first pipeline-.

15. In claim 16, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is configured upon receipt of each token from the store queue, to cause the corresponding data item to be transferred to the memory"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a store queue used when said one of the coprocessor instructions is a store instruction to transfer data items from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and when processing the store instruction places in the store queue the token identifying each of the data items to be transferred, and the partner pipeline stage is in the first pipeline and upon receipt of the token from the store queue, transfers the corresponding data item to the memory-.

16. In claim 18, "A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a load queue used when the coprocessor instruction is a load instruction configured to cause data items to be transferred from memory accessible by the main processor to the coprocessor, the predetermined

pipeline stage is in the first pipeline and is arranged, when processing one of said load instructions, to cause to be placed in the load queue a token identifying each data item to be transferred, and the partner pipeline stage is in the second pipeline and is configured upon receipt of each token from the load queue, to cause the corresponding data item to be transferred to the coprocessor"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein one of the at least one synchronizing queues is a load queue used when said one of the coprocessor instructions is a load instruction to transfer data items from memory accessible by the main processor to the coprocessor, the predetermined pipeline stage is in the first pipeline and when processing the load instruction places in the load queue the token identifying each of the data items to be transferred, and the partner pipeline stage is in the second pipeline and upon receipt of the token from the load queue, transfers the corresponding data item to the coprocessor-.

17. In claim 20, "A data processing apparatus as claimed in Claim 18 wherein one of the at least one synchronizing queues is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is configured upon receipt of each token from the store queue, to cause the corresponding

data item to be transferred to the memory, and wherein the load instruction and store instruction may be vectored coprocessor instructions defining multiple data items to be transferred, and the apparatus further comprises flow control logic, associated with at 1east one of the load queue and the store queue, configured to send a control signal to the predetermined pipeline stage to stop issuance of tokens by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full"

is replaced with -A data processing apparatus as claimed in Claim 18 wherein one of the at least one synchronizing queues is a store queue used when said one of the coprocessor instructions is a store instruction to transfer data items from the coprocessor to the memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and when processing the store instruction places in the store queue the token identifying each of the data items to be transferred, and the partner pipeline stage is in the first pipeline and upon receipt of the token from the store queue, transfers the corresponding data item to the memory, and wherein the load instruction and the store instruction are vectored coprocessor instructions defining multiple data items to be transferred, and the apparatus further comprises flow control logic, associated with at least one of the load queue and the store queue, sending a control signal to the predetermined pipeline stage to stop issuance of the token by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full-.

18. In claim 21, "A data processing apparatus as claimed in Claim 20, wherein the flow control logic is provided for the store queue, the flow control logic being configured to issue the control signal upon receiving an indication from the main processor that the partner pipeline stage cannot accept a data item"

is replaced with -A data processing apparatus as claimed in Claim 20, wherein the flow control logic is provided for the store queue, the flow control logic issuing the control signal upon receiving an indication from the main processor that the partner pipeline stage cannot accept the data item-.

19. In claim 24, "A data processing apparatus as claimed in Claim 1, wherein the main processor is configured, when it is necessary to flush coprocessor instructions from both the first and the second pipeline, to broadcast a flush signal to the coprocessor identifying the tag relating to the oldest instruction that needs to be flushed, the coprocessor being configured to identify that oldest instruction from the tag and to flush from the second pipeline that oldest instruction and any later instructions within the coprocessor"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein the main processor broadcasting, when it is necessary to flush the coprocessor instructions from both the first and the second pipelines, a flush signal to the coprocessor identifying the tag relating to the oldest one of the coprocessor instructions that needs to be flushed, the coprocessor identifying the oldest one of the coprocessor instructions from the tag and flushing from the second pipeline the oldest one of the coprocessor

instructions and any of the coprocessor instructions subsequent to said oldest one of the coprocessor instructions identified within the coprocessor-.

20. In claim 25, "A data processing apparatus as claimed in Claim 24, wherein one or more of said at least one synchronizing queues are flushed in response to said flush signal, with the tag being used to identify which tokens within the queue are to be flushed"

is replaced with -A data processing apparatus as claimed in Claim 24, wherein one or more of said at least one synchronizing queues are flushed in response to said flush signal, with the tag being used to identify which of the tokens within the one or more of the at least one synchronizing queues are to be flushed-.

21. In claim 27, "A data processing apparatus as claimed in Claim 1, wherein a plurality of said coprocessors are provided, with each synchronizing queue coupling a pipeline stage in the main processor with a pipeline stage in one of the coprocessors"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein a plurality of said coprocessors are provided, with each one of the at least one synchronizing queue coupling one of the first plurality of pipeline stages in the main processor with one of the second plurality of pipeline stages in one of the coprocessors-

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22. In claim 28, "A data processing apparatus as claimed in Claim 1, wherein the data processing apparatus has a synchronous design, such that the tokens are caused to be placed in the queue by the predetermined pipeline stage and are caused to be received from the queue by the partner pipeline stage upon changing edges of a clock cycle"

is replaced with -A data processing apparatus as claimed in Claim 1, wherein the data processing apparatus has a synchronous design, such that the token is placed in the at least one synchronizing queue by the predetermined pipeline stage and is received from the at least one synchronizing queue by the partner pipeline stage upon changing edges of a clock cycle-.

23. In claim 29, "A method of synchronization between pipelines in a data processing apparatus, the data processing apparatus comprising a main processor configured to execute a sequence of instructions and a coprocessor configured to execute coprocessor instructions in said sequence of instructions, the main processor comprising a first pipeline having a first plurality of pipeline stages, and the coprocessor comprising a second pipeline having a second plurality of pipeline stages, and each coprocessor instruction being arranged to be routed through both the first pipeline and the second pipeline, the method comprising the steps of:

(a) coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines via a synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries;

(b) placing a token in an entry of the synchronizing queue when the predetermined pipeline stage is processing a coprocessor instruction, the token including a tag which uniquely identifies the coprocessor instruction to which the token relates;

(c) upon receipt of the token from the synchronizing queue by the partner pipeline stage, processing the coprocessor instruction within the partner pipeline stage;

wherein synchronization of the first mid second pipelines between the predetermined pipeline stage and the partner pipeline stage is obtained without passing signals with fixed timing between the pipelines"

is replaced with -A method of synchronization between pipelines in a data processing apparatus comprising the steps of:

executing a sequence of instructions by a main processor having a first pipeline with a first plurality of pipeline stages;

executing coprocessor instructions in said sequence of instructions by a coprocessor having a second pipeline with a second plurality of pipeline stages, wherein each of the coprocessor instructions being arranged to be routed through both the first pipeline and the second pipeline;

(a) coupling a predetermined pipeline stage in one of the first or second pipeline with a partner pipeline stage in the other one of the first or second pipeline via a synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries;

(b) placing a token in an entry of the synchronizing queue when the predetermined pipeline stage is processing one of the coprocessor instructions, the token including a tag which uniquely identifies said one of the coprocessor instructions to which the token relates;

(c) upon receipt of the token from the synchronizing queue by the partner pipeline stage, processing the corresponding one of the coprocessor instructions within the partner pipeline stage;

synchronizing the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage without passing signals with fixed timing between the first and second pipelines-.

24. In claim 30, "A method as claimed in Claim 29, wherein a plurality of said synchronizing queues are provided, and said steps (a) to (c) are performed for each synchronizing queue"

is replaced with -A method as claimed in Claim 29 further comprising performing said steps (a) to (c) for each of a plurality of said synchronizing queues-.

25. In claim 31, "A method as claimed in Claim 29, wherein one of the at least one synchronizing queues is an instruction queue, the predetermined pipeline stage is in the first pipeline and the partner pipeline stage is in the second pipeline, the method comprising the steps of:

at said step (b), placing a token in the instruction queue identifying a coprocessor instruction; and

at said step (c), upon receipt of the token, beginning processing of the coprocessor instruction identified by the token within the partner pipeline stage"

is replaced with -A method as claimed in Claim 29 further comprising the steps of:

at said step (b), wherein the synchronizing queue is an instruction queue, the predetermined pipeline stage in the first pipeline places the token in the instruction queue identifying said one of the coprocessor instructions; and

at said step (c), upon receipt of the token, beginning processing of the corresponding one of the coprocessor instructions identified by the token within the partner pipeline stage in the second pipeline-.

26. In claim 32, "A method as claimed in Claim 29, wherein one of the at least one synchronizing queues is a cancel queue, the predetermined pipeline stage is in the first pipeline and the partner pipeline stage is in the second pipeline, the method comprising the steps of:

at said step (b), placing a token in the cancel queue identifying whether a coprocessor instruction at that predetermined pipeline stage is to be cancelled; and

at said step (c), upon receipt of the token from the cancel queue by the partner pipeline stage, and if the token identifies that the coprocessor instruction is to be cancelled, causing that coprocessor instruction to be cancelled"

is replaced with -A method as claimed in Claim 29 further comprising the steps of:

at said step (b), wherein the synchronizing queue is a cancel queue, the predetermined pipeline stage in the first pipeline places the token in the cancel queue identifying whether said one of the coprocessor instructions at the predetermined pipeline stage is to be cancelled; and

at said step (c), upon receipt of the token from the cancel queue by the partner pipeline stage in the second pipeline, and if the token identifies that said one of the coprocessor instructions is to be cancelled, cancelling the corresponding one of the coprocessor instructions-.

27. In claim 33, "A method as claimed in Claim 29, wherein one of the at least one synchronizing queues is a finish queue, the predetermined pipeline stage is in the first pipeline and the partner pipeline stage is in the second pipeline, the method comprising the steps of:

at said step (b), placing in the finish queue a token identifying permission for a coprocessor instruction at that predetermined pipeline stage to be retired from the second pipeline; and

at said step (c), upon receipt of the token from the finish queue by the partner pipeline stage, and if the token identifies that the coprocessor instruction is permitted to be retired, causing that coprocessor instruction to be retired"

is replaced with -A method as claimed in Claim 29 further comprising the steps of:

at said step (b), wherein the synchronizing queue is a finish queue, the predetermined pipeline stage in the first pipeline places in the finish queue the token identifying permission for said one of the coprocessor instructions at said predetermined pipeline stage to be retired from the second pipeline; and

at said step (c), upon receipt of the token from the finish queue by the partner pipeline stage in the second pipeline, and if the token identifies that said one of the coprocessor instructions is permitted to be retired, retiring the corresponding one of the coprocessor instructions-.

28. In claim 34, "A method as claimed in Claim 29, wherein one of the at least one synchronizing queues is a length queue, the predetermined pipeline stage is in the second pipeline and the partner pipeline stage is in the first pipeline, and the method comprises the steps of:

at said step (b), for a vectored coprocessor instruction, placing in the length queue a token identifying length information for the vectored coprocessor instruction; and

at said step (c), upon receipt of the token from the length queue by the partner pipeline stage, factoring the length information into the further processing of the vectored coprocessor instruction within the first pipeline"

is replaced with -A method as claimed in Claim 29 further comprises the steps of:

at said step (b), wherein the synchronizing queue is a length queue, the predetermined pipeline stage in the second pipeline places in the length queue the token identifying length information for a vectored coprocessor instruction; and

at said step (c), upon receipt of the token from the length queue by the partner pipeline stage in the first pipeline, factoring the length information into the further processing of the vectored coprocessor instruction within the first pipeline-.

29. In claim 35, "A method as claimed in Claim 29, wherein one of the at least one synchronizing queues is an accept queue, the predetermined pipeline stage is in the second pipeline and the partner pipeline stage is in the first pipeline, the method comprising the steps of:

at said step (b), placing in the accept queue a token identifying whether a coprocessor instruction in that predetermined pipeline stage is to be accepted for execution by the coprocessor; and

at said step (c), upon receipt of the token from the accept queue by the partner pipeline stage, and if the token identifies that the coprocessor instruction is not to be accepted, causing that coprocessor instruction to be rejected by the main processor"

is replaced with -A method as claimed in Claim 29 further comprising the steps of:

at said step (b), wherein the synchronizing queue is an accept queue, the predetermined pipeline stage in the second pipeline places in the accept queue the

token identifying whether said one of the coprocessor instructions in said predetermined pipeline stage is to be accepted for execution by the coprocessor; and

at said step (c), upon receipt of the token from the accept queue by the partner pipeline stage in the first pipeline, and if the token identifies that said one of the coprocessor instructions is not to be accepted, rejecting the corresponding one of the coprocessor instructions by the main processor-.

30. In claim 36, "A method as claimed Claim 29, wherein one of the at least one synchronizing queries is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and the partner pipeline stage is in the first pipeline, the method comprising the steps of:

at said step (b), when processing one of said store instructions, placing in the store queue a token identifying each data item to be transferred; and

at said step (c), upon receipt of each token from the store queue by the partner pipeline stage, causing the corresponding data item to be transferred to the memory"

is replaced with -A method as claimed Claim 29 further comprising the steps of:

processing said one of the coprocessor instructions including a store instruction for transferring data items from the coprocessor to memory accessible by the main processor;

at said step (b), wherein the synchronizing queue is a store queue, when processing said store instruction, the predetermined pipeline stage in the second pipeline places in the store queue the token identifying each of the data items to be transferred; and

at said step (c), upon receipt of the token from the store queue by the partner pipeline stage in the first pipeline, transferring the corresponding data item to the memory-.

31. In claim 37, "A method as claimed in claim 29, wherein one of the at least one synchronizing queues is a load queue used when the coprocessor instruction is a load instruction configured to cause data items to be transferred from. memory accessible by the main processor to the coprocessor, the predetermined pipeline stage is in. the first pipeline and the partner pipeline stage is in the second pipeline, the method comprising the steps of:

at said step (b), when processing one of said load instructions, placing in the load queue a token identifying each data item to be transferred; and

at said step (c), upon receipt of each token from the load queue by the partner pipeline stage, causing the corresponding data item to be transferred to the coprocessor"

is replaced with -A method as claimed in claim 29, further comprising the steps of:

processing said one of the coprocessor instructions including a load instruction for transferring data items from memory accessible by the main processor to the coprocessor;

at said step (b), wherein the synchronizing queue is a load queue, when processing the load instruction, the predetermined pipeline stage in the first pipeline places in the load queue the token identifying each of the data items to be transferred; and

at said step (c), upon receipt of the token from the load queue by the partner pipeline stage in the second pipeline, transferring the corresponding data item to the coprocessor-.

32. In claim 38, "A method as claimed in Claim 37 wherein one of the at least one synchronizing queues is a store queue used when the coprocessor instruction is a store instruction configured to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and the partner pipeline stage is in the first pipeline, the method comprising the steps of:

at said step (b), when processing one of said store instructions, placing in the store queue a token identifying each data item to be transferred; and

at said step (c), upon receipt of each token from the store queue by the partner pipeline stage, causing the corresponding data item to be transferred to the memory; and

wherein the load instruction and store instruction may be vectored coprocessor instructions defining multiple data items to be transferred, and the method further comprises the step of:

(d) for at least one of the load queue and the store queue, sending a control signal to the predetermined pipeline stage to stop issuance of tokens by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full"

is replaced with -A method as claimed in Claim 37 further comprising the steps of:

processing said one of the coprocessor instructions including a store instruction for transferring data items from the coprocessor to the memory accessible by the main processor;

at said step (b), wherein the synchronizing queue is a store queue, when processing one of said store instructions, the predetermined pipeline stage in the second pipeline places in the store queue the token identifying each of the data items to be transferred; and

at said step (c), upon receipt of the token from the store queue by the partner pipeline stage in the first pipeline, transferring the corresponding data item to the memory; and

defining multiple data items to be transferred when the load instruction and the store instruction are vectored coprocessor instructions, and the method further comprises the step of:

(d) for at least one of the load queue and the store queue, sending a control signal to the predetermined pipeline stage to stop issuance of the token by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full-.

33. In claim 39, "A method as claimed in Claim 38, wherein said step (d) is performed for the store queue, at said step (d) the method comprising the step of issuing the control signal upon receiving an indication from the main processor that the partner pipeline stage cannot accept a data item"

is replaced with -A method as claimed in Claim 38 further comprising the steps of: at said step (d), when said step (d) is performed for the store queue, issuing the control signal upon receiving an indication from the main processor that the partner pipeline stage cannot accept the data item-.

34. In claim 41, "A method as claimed in Claim 29, wherein, when it is necessary to flush coprocessor instructions from both the first and the second pipeline, the method further comprises the steps of:

broadcasting a flush signal from the main processor to the coprocessor identifying the tag relating to the oldest instruction that needs to be flushed;

within the coprocessor, identifying from the tag that oldest instruction and flushing from the second pipeline that oldest instruction and any later instructions within the coprocessor"

is replaced with -A method as claimed in Claim 29 further comprising the steps of:

when it is necessary to flush the coprocessor instructions from both the first and the second pipelines, broadcasting a flush signal from the main processor to the coprocessor identifying the tag relating to the oldest one of the coprocessor instructions that needs to be flushed; and

within the coprocessor, when it is necessary to flush the coprocessor instructions from both the first and the second pipelines, identifying from the tag the oldest one of the coprocessor instructions and flushing from the second pipeline the oldest one of the coprocessor instructions and any of the coprocessor instructions subsequent to said oldest one of the coprocessor instructions identified within the coprocessor-.

35. In claim 42, "A method as claimed in Claim 4I, further comprising the step of flushing one or more of said at least one synchronizing queues in response to said flush signal, with the tag being used to identify which tokens within the queue are to be flushed"

is replaced with -A method as claimed in Claim 4I, further comprising the step of flushing the synchronizing queue in response to said flush signal, with the tag being used to identify which of the tokens within the synchronizing queue are to be flushed-.

36. In claim 44, "A method as claimed in Claim 29, wherein a plurality of said coprocessors are provided, with each synchronizing queue coupling a pipeline stage in the main processor with a pipeline stage in one of the coprocessors"

is replaced with -A method as claimed in Claim 29, wherein a plurality of said coprocessors are provided, further comprising the steps of coupling one of the first plurality of pipeline stages in the main processor with one of the second plurality of pipeline stages in one of the coprocessors via the synchronizing queue-.

37. In claim 45, "A method as claimed in Claim 29, wherein the data processing apparatus has a synchronous design, such that the tokens are placed in the queue by the predetermined pipeline stage and are received from the queue by the partner pipeline stage upon changing edges of a clock cycle"

is replaced with -A method as claimed in Claim 29 further comprising the steps of placing the token in the synchronizing queue by the predetermined pipeline stage and receiving the token from the synchronizing queue by the partner pipeline stage upon changing edges of a clock cycle for having a synchronous design-.

II. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

38. Claims 1-22, 24-25, 27-39, 41-42 and 44-45 are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

39. The primary reasons for allowance of claim 1 in the instant application is the combination with the inclusion in the claim that there are "**A data processing apparatus, comprising:**

a main processor that executes a sequence of instructions, the main processor comprising a first pipeline having a first plurality of pipeline stages;

a coprocessor that executes coprocessor instructions in said sequence of instructions, the coprocessor comprising a second pipeline having a second plurality of pipeline stages, and each one of the coprocessor instructions being arranged to be routed through both the first pipeline and the second pipeline; and

at least one synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries and coupling a predetermined pipeline stage in one of the first or second pipeline with a partner pipeline stage in the other one of the first or second pipeline, the predetermined pipeline stage placing a token in an entry of the synchronizing queue when processing one of the coprocessor instructions, the token including a tag which uniquely identifies said one of the coprocessor instructions to which the token relates, and the partner pipeline stage processing the corresponding one of the coprocessor instructions upon receipt of the token from the synchronizing queue, thereby synchronizing the first and second pipelines between the predetermined pipeline stage and the

partner pipeline stage without passing signals with fixed timing between the first and second pipelines" The prior art of record including the disclosures of Gearty (US Patent 6,477,638) and Martin et al. (US Patent 6,381,692) neither anticipates nor renders obvious the above recited combination. Because claims 2-22, 24-25 and 27-28 depend directly or indirectly on claim 1, these claims are considered allowable for at least the same reasons noted above.

40. The primary reasons for allowance of claim 29 in the instant application is the combination with the inclusion in the claim that there are "**A method of synchronization between pipelines in a data processing apparatus comprising the steps of:**

executing a sequence of instructions by a main processor having a first pipeline with a first plurality of pipeline stages;

executing coprocessor instructions in said sequence of instructions by a coprocessor having a second pipeline with a second plurality of pipeline stages, wherein each of the coprocessor instructions being arranged to be routed through both the first pipeline and the second pipeline;

(a) coupling a predetermined pipeline stage in one of the first or second pipeline with a partner pipeline stage in the other one of the first or second pipeline via a synchronizing queue including a first-in-first-out (FIFO) buffer having a predetermined plurality of entries;

(b) placing a token in an entry of the synchronizing queue when the predetermined pipeline stage is processing one of the coprocessor instructions, the token including a tag which uniquely identifies said one of the coprocessor instructions to which the token relates;

(c) upon receipt of the token from the synchronizing queue by the partner pipeline stage, processing the corresponding one of the coprocessor instructions within the partner pipeline stage;

synchronizing the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage without passing signals with fixed timing between the first and second pipelines" The prior art of record including the disclosures of Gearty (US Patent 6,477,638) and Martin et al. (US Patent 6,381,692) neither anticipates nor renders obvious the above recited combination. Because claims 28-39, 41-42 and 44-45 depend directly or indirectly on claim 29, these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

October 06, 2008

Chun-Kuan (Mike) Lee
Examiner
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/Alford W. Kindred/

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